


U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1987		SERIAL NO. 10/098,639			
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Robert Kerr et al.			
FILING DATE March 12, 2002				GROUP 2825			
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
CL	AA 4,516,147	05/07/85	Komatsu et al.	—	—		
CL	AB 6,008,094	12/28/99	Krivokapic et al.	—	—		
	AC						
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1987		SERIAL NO. 10/098,659	
 LIST OF ART CITED BY APPLICANT (Attach several sheets if necessary)				APPLICANT Robert Kerr et al.		FILING DATE March 12, 2002	
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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Eating Date If Appropriate	
CL	AA 5,965,924	10/12/1999	Yen	—	—		
CL	AB 5,278,082	1/11/1994	Kawamura	—	—		
CL	AC 6,242,781 B1	6/5/2001	Batra et al.	—	—		
CL	AD 5,895,939	4/20/1999	Ueno	—	—		
CL	AE 5,838,068	11/17/1998	Tang	—	—		
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
CL	AA	5,166,096		Cote et al.			
	AB	5,814,886	09/98	Mano			
	AC	5,895,269	04/99	Wang et al.			
	AD	5,600,170	02/97	Sugiyama et al.			
	AE	5,990,524	11/99	En et al.			
	AF	5,874,359	02/99	Liaw et al.	438	640	
	AG	5,707,883	01/98	Tabara	437	40	
	AH	5,686,331	11/97	Song	437	41	
	AI	5,960,318	09/99	Peschke et al.	438	637	
	AJ	5,747,359	05/98	Yuan et al.	437	186	
	AK	5,946,578	08/99	Fujii	438	300	
CL	AL	5,763,321	06/98	Ohsima et al.	438	618	
FOREIGN PATENT DOCUMENTS							
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
CL	AR		Shenai, K., "A high-density, self-aligned power MOSFET structure fabricated using sacrificial spacer technology" Electron Devices, IEEE Transactions on Electron Devices, Vol. 39, Issue 5, May 1992, pgs. 1252-1255				
CL	AS		Wolf, S. "Silicon Processing for the VLSI Era," Vol. 3: The Submicron MOSFET, Lattice Press 1995, pgs. 634-636.				
CL	AT		Stanley Wolf, Ph.D., "Silicon Processing for the VLSI Era," Volume 3: The Submicron MOSFET, Lattice Press, 1995, pgs. 136-138 and 232-234				
EXAMINER calorula				DATE CONSIDERED 12.22.95			
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U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
U	AA	5,206,187	04/93	Doan et al.	437	192	
	AB	5,731,610	03/98	Rhodes	257	309	
	AC	5,162,890	11/92	Butler	257	306	
		5,173,752	12/92	Motonami et al.	257	309	
	AE	5,272,367	12/93	Dennison et al.	257	306	
	AF	5,317,193	05/94	Watanabe	257	774	
	AG	5,444,003	08/95	Wang et al.	437	31	
	AH	5,510,648	04/96	Davies et al.	257	657	
	AI	5,547,892	08/96	Wuu et al.	437	52	
	AJ	5,552,620	09/96	Lu et al.	437	195	
U	AK	5,612,240	03/97	Chang	437	44	
	AL						
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	AR		Gray & Meyer, "Analysis and Design of Analog Integrated Circuits", Third Edition, John Wiley & Sons, Inc., 1993, pg. 169				
	AS						
	AT						
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U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
CL	AA	5,652,174	07/97	Wuu et al.	437	60		
	AB	5,668,021	09/97	Subramanian et al.	438	282		
	AC	5,710,450	01/98	Chau et al.	257	344		
	AD	5,736,441	04/98	Chen	438	255		
	AE	5,808,320	09/98	Dennison	257	68		
	AF	5,811,350	09/98	Dennison	438	597		
	AG	5,885,890	03/99	Dennison	438	597		
	AH	5,243,219	09/93	Katayama	287	740		
	AI	5,912,492	06/99	Chang et al.	257	344		
	AJ	5,897,350	04/99	Lee et al.	438	238		
	AK	5,891,780	04/99	Hasegawa et al.	438	278		
CL	AL	5,864,155	01/99	Melzner	257	306		
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CL	AA	4,281,448	08/81	Barry et al.	29	577	
	AB	5,930,618	07/99	Sun et al.	438	240	
	AC	5,591,662	01/97	Zambrano	437	57	
	AD	5,899,712	05/99	Choi et al.	438	163	
	AE	4,936,928	06/90	Shaw et al.	148	33.4	
	AF	5,970,360	10/99	Cheng et al.	438	398	
	AG	5,858,832	01/99	Pan	438	230	
	AH	5,866,927	02/99	Cho et al.	257	296	
	AI	5,895,269	04/99	Wang et al.	438	675	
	AJ	6,093,609	07/00	Chuang	438	286	
	AK	6,133,103	10/00	Lee et al.	438	276	
CL	AL	6,097,103	08/00	Ishigaki	257	903	
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